

WHAT IS CLAIMED IS:

1. A method for manufacturing multi-level interconnection lines of semiconductor device comprising:
 - 5 forming a first interconnection line on a semiconductor substrate;
 - forming a first interlayer insulating layer on the first interconnection line;
 - 10 forming a first etching stop layer on the first interlayer insulating layer;
 - forming a via hole exposing the first interconnection line by selectively etching the first etching stop layer and the first interlayer insulating layer;
 - 15 forming etching stop patterns around an inlet of the via hole by selectively etching the first etching stop layer;
 - forming a second interlayer insulating layer on the etching stop pattern and the first interlayer insulating layer;
 - 20 forming a trench by selectively etching the second interlayer insulating layer; and
 - forming a conductive layer in the trench and in the via hole.
- 25 2. The method of claim 1, wherein the method further comprises:
 - 30 forming a photoresist pattern around the inlet of the via hole to cover portions of the first etching stop layer; and
 - removing other portions of the first etching stop layer which are not covered with the photoresist pattern, whereby the etching stop patterns are formed.

3. The method of claim 1, wherein the method further comprises:

5 forming a third interlayer insulating layer on the semiconductor substrate;

forming a second etching stop layer on the third interlayer insulating layer;

10 patterning the second etching stop layer and the third interlayer insulating layer to expose an opening; and

15 forming a conductive layer in the opening whereby the first interconnection line is formed.

4. The method of claim 1, wherein the trench exposes portions of the etching stop patterns at the bottom thereof.

20 5. The method of claim 1, wherein the width of the trench is wider than that of the via hole.

6. The method of claim 1, wherein a void is formed within the via hole in the step of forming the second interlayer insulating layer.

25 7. The method of claim 6, wherein the second interlayer insulating layer is formed with any one selected from the group consisting of an USG layer deposited by the high density plasma, an oxide deposited by plasma enhance chemical vapor deposition method or low 30 pressure chemical vapor deposition.

8. The method of claim 6, wherein the second interlayer insulating layer is formed at a thickness ranging from about 3000 Å to about 30000 Å.

5 9. The method of claim 1, wherein the first interlayer insulating layer is formed with any one selected from the group consisting of a spin on glass layer, an oxide layer deposited by a plasma enhance chemical vapor deposition method, an oxide layer 10 deposited by a high density plasma method and a tetra-ethyl-ortho-silicate(TEOS) layer.

15 10. The method of claim 9, the first interlayer insulating layer is formed at a thickness ranging from about 2000 Å to about 30000 Å.

11. The method of claim 1, wherein the first etching stop layer is formed with any one selected from the group consisted of a nitride layer deposited by a plasma 20 enhance chemical vapor deposition method, a SiON layer, a Ta₂O₅ layer, a ZnO₂ layer, a ZrO₂ layer, a ZnO layer, a HfO layer and an Al₂O₃ layer.

12. The method of claim 11, wherein the first 25 etching stop layer is formed at a thickness ranging from about 200 Å to about 3000 Å.

13. The method of claim 1, wherein the first 30 interconnection line is formed of any one selected form a group consisting of Al, Cu, Au, Ag and Cr.

14. The method of claim 1, the first interconnection line is formed at a thickness ranging from about 2000 Å to about 30000 Å.

5 15. A Semiconductor device made in accordance with the method of claim 1.

16. A Semiconductor device made in accordance with the method of claim 2.

10

17. A Semiconductor device made in accordance with the method of claim 3.

15

18. A Semiconductor device made in accordance with the method of claim 7.

19. A Semiconductor device made in accordance with the method of claim 9.

20

20. A Semiconductor device made in accordance with the method of claim 11.